Chapter 37 Class G Power Amplifier

Class G power amplifier is similar to Class B power amplifier. Fig. 37-1 shows the schematic diagram of Class G power amplifier.

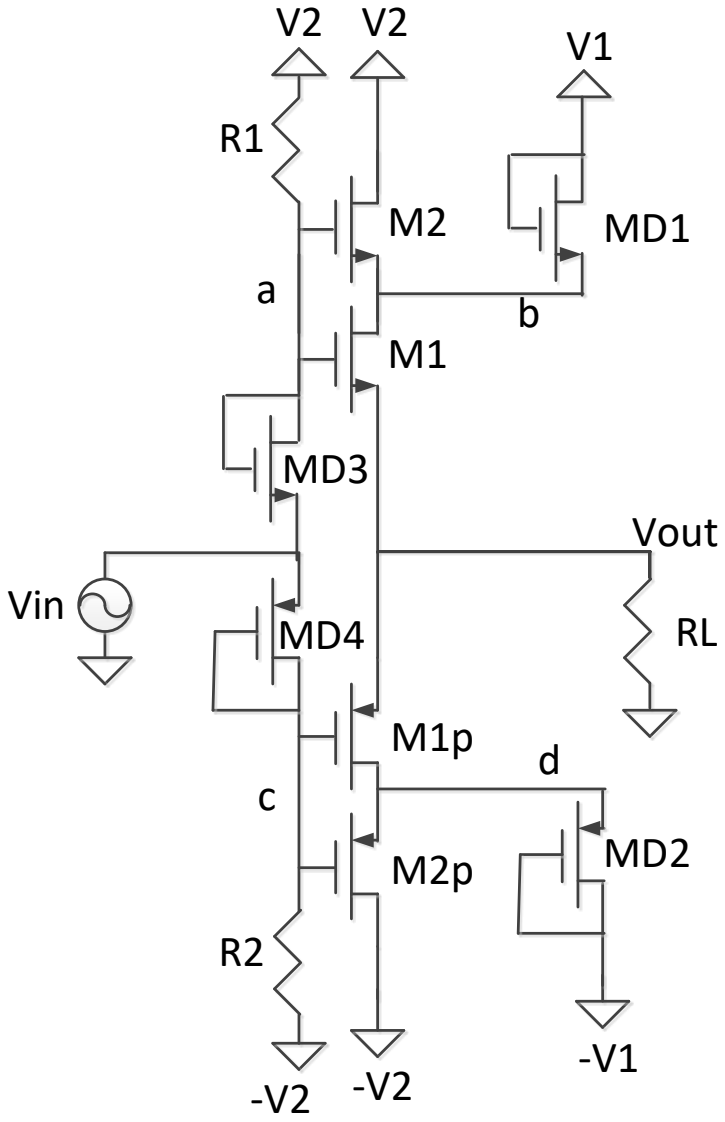

Fig. 37-1 A schematic diagram of Class G power amplifier

In the circuit shown in Fig. 37-1, the following needs to be noted.

(1) There are two power supplies: V1 and V2. V1 is a small power supply while V2 is a larger power supply.
(2) M2 and M1 are NMOS transistors while M1p and M2p are PMOS transistors.

(3) MD1 to MD4 are all transistors connected as diodes.
(4) The input Vin is a sinusoidal signal centered at 0.

The Class G power amplifier is designed to save energy. The circuit works as follows:

(1) When Vin is positive, M1p and M2p are both cut off and M1 and M2 will be conducting.
(2) If Vin is positive and small, V2 power supply will be cut off and only M1 will be conducting. Thus V1, which is a small power supply, is used in this case.
(3) If Vin is positive and large, V1 power supply will be cut off and M2 and M1 will be conducting. Thus V2, which is a large power supply, is used in this case
(4) When Vin is negative, M1 and M2 are both cut off and M1p and M2p will be conducting.
(5) If Vin is negative and small, -V2 will be cut off and only M1p will be conducting. Thus only –V1, which is a small power supply, is used in this case.
(6) If Vin is negative and large, -V1 will be cut off and M2p and M1p will be conducting. Thus only -V2, which is a large power supply, is used in this case.

From the above discussion, we can see that Class G power amplifier is an improved version of Class B power amplifier. The amplitude of Vin can be quite large for Class G power amplifier. Therefore a large power supply needs to be used. It is important that this large power supply is used only when Vin is large in amplitude.

In the following, we will explain in detail how the circuit works. Consider Fig. 37-2.

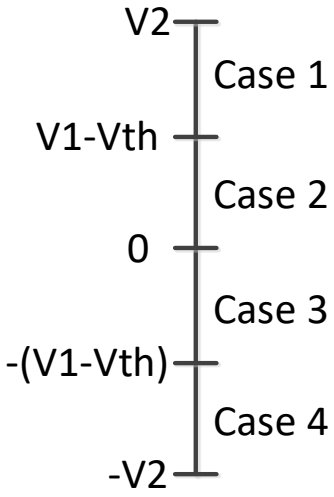

Fig. 37-2 The four cases of Vin

We first note the following:

(1) $Va = Vin + Vth$. (37-1)

(2) $Vb = V1 - Vth$. (37-2)

Case 1 in Fig. 37-2.

In this case, Vin satisfies the following condition:

$(V1 - Vth) < Vin < V2$. (37.3)

$VGS2 = Va - Vb = Vin - V1 + 2Vth = Vin - (V1 - Vth) + Vth$. (37-4)

Let $P = Vin - (V1 - Vth)$ (37-5)

Since we assume that Vin is larger than V1-Vth, P is positive. From Equation (37-4), we have

$VGS2 = P + Vth > Vth$ (37-6)

and M2 will conduct in this case. That is, M2 conducts when

$Vin > V1 - Vth$. (37-7)

As soon as M2 conducts, Vb will rise, MD1 will be reversely biased and V1 will be blocked. That is, only V2 is used in this case. Note that since M2 conducts, M1 must also conduct. We now discuss why current can flow in M1.

The condition for M1 to conduct is as follows:

$$VGS1 = Va - Vout = Vin + Vth - Vout > Vth \tag{37-8}$$

Thus we must make sure that Vin is larger than or equal to Vout. This can be achieved by carefully adjusting parameters of the circuit.

We may summarize Case 1 as follows:

(1) V1 is blocked and V2 is used.
(2) M2 and M1 both conduct.
(3) Current flows from V2 through M2 and M1 to RL

Case 2 in Fig. 37-2.

In this case, Vin satisfies the following condition:

$$0 < Vin < (V1 - Vth). \tag{37-9}$$

It can be easily seen that under such condition, we will have:

$$VGS2 = P + Vth < Vth, \tag{37-10}$$

because P is negative. Thus M2 will be cut off, V2 will not be used. .

The discussion about M1 in Case 1 is still valid in Case 2. Thus only M1 conducts and V1 is used. We therefore may summarize Case 2 as follows:

(1) V2 is cut off and V1 is used.
(2) Only M1 conducts.
(3) Current flows from V1 through M1 to RL.

As for Cases 3 to4, note that in these two acses, Vin is below 0. Since the circuit

in Fig. 37-1 is symmetrical, by slightly modifying the discussion of Cases 1 to 2, we can show that M2p will conduct only when the absolute value of the amplitude of Vin is large.

In the following section, we will conduct some experiments of the Class G power amplifier circuit shown in Fig. 37-1.

Section 37.1 Testing of the Class G Power Amplifier Circuit

Experiment 37.1-1 The First Test of the Class G Power Amplifier Circuit Shown in Fig. 37-1.

In this test, the circuit is the one shown in Fig. 37-1. The program is in Table 37.1-1 and the results are in Fig. 37.1-1. Some important parameters are shown below.

R1=R2=5K
V2=5V
V1=3V
All transistors are power transistors
Vth=2V for all transistors
RL=50
Vin amplitude=1.5V, DC=0, frequency=3KHz

Table 37.1-1 The program for Experiment 37.1-1

```
amplifier
.protect
.lib "C:\model\tsmc\MIXED035\mm0355v.l" TT
.unprotect
.op
.options nomod post

V1   V1   0    3v
V2   V2   0    5v
V1p  V1p  0    -3v
V2p  V2p  0    -5v

R1   V2   a    5K
R2   V2p  c    5K

M1   b    a    OUT V2p  M2N6802      W=2u L=2u
M2   V2   a    b    V2p  M2N6802      W=4u L=2u
```

```
M1p     d    c    OUT V2   M2N6804     W=2u L=2u
M2p     V2p  c    d    V2   M2N6804     W=4u L=2u

MD1     V1   V1   b    V2p  M2N6802     W=4u L=2u
MD2     V1p  V1p  d    V2   M2N6804     W=4u L=2u
MD3     a    a    IN   V2p  M2N6802     W=2u L=2u
MD4     c    c    IN   V2   M2N6804     W=2u L=2u

RL   OUT 0    50

.model M2N6802   NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
Vmax=0 Xj=0
+          Tox=100n Uo=600 Phi=.6 Rs=.1084 Kp=20.88   Vto=2 NSUB=1E15
+          Rd=1.163   Cbd=732p Pb=.8 Mj=.5 Fc=.5 Cgso=1.725n
+          Cgdo=136.7p   Is=1.823p N=1 Tt=2060n)

.model M2N6804   PMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
Vmax=0 Xj=0
+          Tox=100n Uo=300 Phi=.6 Rs=.153 Kp=10.46 Vto=-2 NSUB=1E15
+          Rd=66.52m   Cbd=1.281n Pb=.8 Mj=.5 Fc=.5 Cgso=1.798n
+          Cgdo=134.9p   Is=5.477p N=3 Tt=295n)

Vin  IN   0    sin(0V 1.5V 3K)

.tran 0.1us 0.6ms
.probe TRAN I(M1) I(M2) I(M1p) I(M2p) power=PAR('V(OUT)*I(RL)')

.end
```

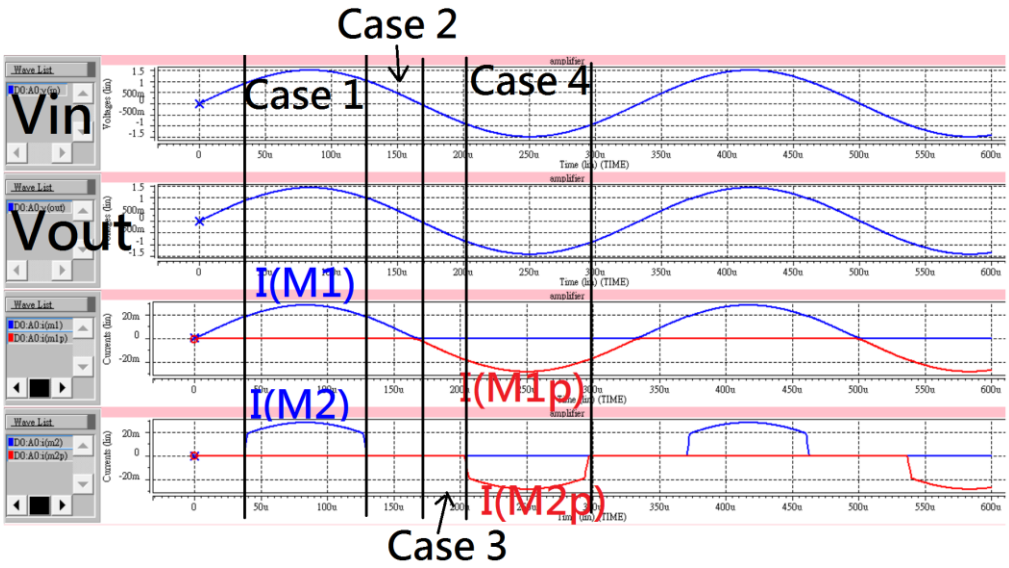

Fig. 37.1-1 The results of Experiment 37.1-1

From Fig. 37.1-1, we can see the following:

(1) Only M1 and M2 conduct when Vin is positive.
(2) Only M1p and M2P conduct when Vin is negative.
(3) M2 and M2p conduct only when the amplitude of Vin assumes large value.
(4) V1=3 and Vth=2. V1-Vth=3-2=1. M2 is turned on when Vin is larger than 1V which is predicted by Equation (37-7).
(5) Vout amplitude=1.5V, DC=0, frequency=3KHz

In summary, the experimental results of Experiment 37.1-1 show that the circuit in Fig. 37-1 works as a Class G power amplifier and validates the discussion about the circuit at the beginning of this chapter.

Section 37.2 More Experiments

Class G power amplifiers are often used in audio systems. Therefore we like to know whether the amplifier discussed in this chapter can handle signal with frequency up to 100KHz.

Experiment 37.2-1 Increasing Input Frequency from 3kHz to 1000Kz

In this experiment, we increase the input frequency from 3KHz to 100KHz. The program is in Table 37.2-1 and the results are in Fig. 37.2-1. As can be seen, the circuit works well for this frequency.

Table 37.2-1 The program for Experiment 27.2-1

```
amplifier
.protect
.lib "C:\model\tsmc\MIXED035\mm0355v.l" TT
.unprotect
.op
.options nomod post

V1   V1   0    3v
V2   V2   0    5v
V1p  V1p  0    -3v
V2p  V2p  0    -5v

R1   V2   a    5K
R2   V2p  c    5K

M1   b    a    OUT V2p  M2N6802      W=2u L=2u
M2   V2   a    b   V2p  M2N6802      W=4u L=2u
M1p       d    c   OUT V2   M2N6804      W=2u L=2u
M2p       V2p  c   d   V2   M2N6804      W=4u L=2u

MD1       V1   V1  b   V2p  M2N6802      W=4u L=2u
MD2       V1p  V1p d   V2   M2N6804      W=4u L=2u
MD3       a    a   IN  V2p  M2N6802      W=2u L=2u
MD4       c    c   IN  V2   M2N6804      W=2u L=2u
```

```
RL    OUT 0      50

.model M2N6802    NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
Vmax=0 Xj=0
+             Tox=100n Uo=600 Phi=.6 Rs=.1084 Kp=20.88     Vto=2 NSUB=1E15
+             Rd=1.163     Cbd=732p Pb=.8 Mj=.5 Fc=.5 Cgso=1.725n
+             Cgdo=136.7p     Is=1.823p N=1 Tt=2060n)

.model M2N6804    PMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
Vmax=0 Xj=0
+             Tox=100n Uo=300 Phi=.6 Rs=.153 Kp=10.46 Vto=-2 NSUB=1E15
+             Rd=66.52m     Cbd=1.281n Pb=.8 Mj=.5 Fc=.5 Cgso=1.798n
+             Cgdo=134.9p     Is=5.477p N=3 Tt=295n)

Vin   IN     0      sin(0V 1.5V 100K)

.tran 0.1us 0.6ms
.probe TRAN I(M1) I(M2) I(M1p) I(M2p) power=PAR('V(OUT)*I(RL)') V(a,b) V(c,d)
V(a,OUT) V(c,OUT)

.end
```

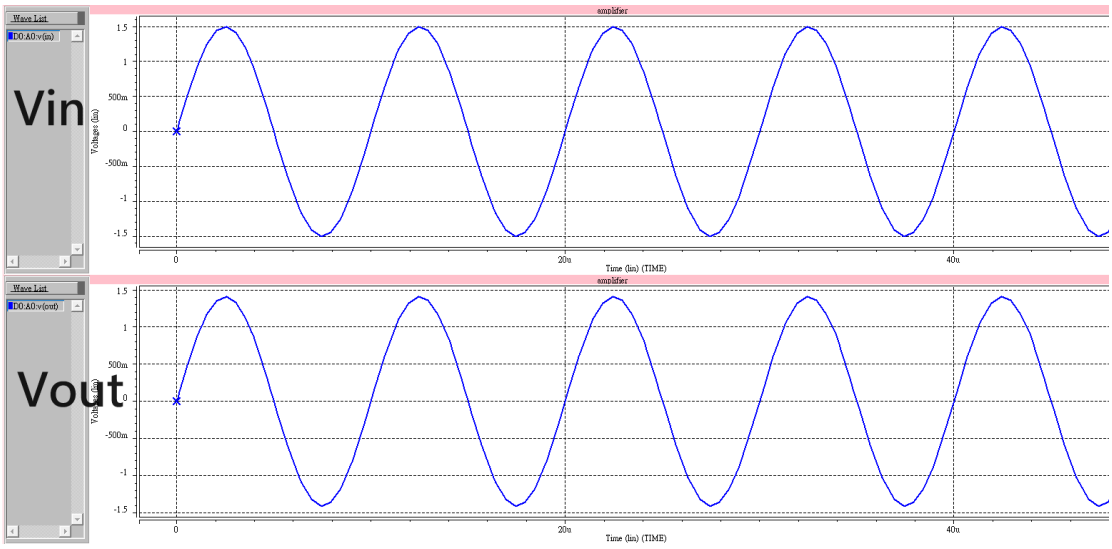

Fig. 37.2-1 The results of Experiment 37.2-1

In the previous experiments, we used power transistors which allow large current

to flow. In the following experiment, we will use ordinary transistors to see whether the circuit will work.

Experiment 37.2-2 Using Ordinary Transistors

In this experiment, we used ordinary transistors. In order to allow large current to flow, we actually used 60 transistors in parallel. The program is in Table 37.2-2 and the results are in Fig. 37.2-2. As can be seen, the amplitude of Vout decreased from 1.5V to 0.3V. Besides, Vout is distorted. Thus, ordinary transistors cannot be used for Class G power amplifier.

Table 37.2-2 The program for Experiment 37.2-2

```
amplifier
.protect
.lib "C:\model\tsmc\MIXED035\mm0355v.l" TT
.unprotect
.op
.options nomod post

V1   V1   0    3v
V2   V2   0    5v
V1p  V1p  0    -3v
V2p  V2p  0    -5v

R1   V2   a    5K
R2   V2p  c    5K

M1   b    a    OUT V2p  NCH W=2u L=2u m=60
M2   V2   a    b   V2p  NCH W=4u L=2u m=60
M1p       d    c   OUT V2   PCH W=2u L=2u m=60
M2p       V2p  c   d   V2   PCH W=4u L=2u m=60

MD1       V1   V1  b   V2p  NCH W=4u L=2u m=60
MD2       V1p  V1p d   V2   PCH W=4u L=2u m=60
MD3       a    a   IN  V2p  NCH W=2u L=2u m=60
MD4       c    c   IN  V2   PCH W=2u L=2u m=60

RL   OUT 0    50
```

```
.model M2N6802    NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
Vmax=0 Xj=0
+          Tox=100n Uo=600 Phi=.6 Rs=.1084 Kp=20.88    Vto=2 NSUB=1E15
+          Rd=1.163    Cbd=732p Pb=.8 Mj=.5 Fc=.5 Cgso=1.725n
+          Cgdo=136.7p    Is=1.823p N=1 Tt=2060n)

.model M2N6804    PMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
Vmax=0 Xj=0
+          Tox=100n Uo=300 Phi=.6 Rs=.153 Kp=10.46 Vto=-2 NSUB=1E15
+          Rd=66.52m    Cbd=1.281n Pb=.8 Mj=.5 Fc=.5 Cgso=1.798n
+          Cgdo=134.9p    Is=5.477p N=3 Tt=295n)

Vin   IN    0     sin(0V 1.5V 100K)

.tran 0.1us 0.6ms
.probe TRAN I(M1) I(M2) I(M1p) I(M2p) power=PAR('V(OUT)*I(RL)') V(a,b) V(c,d)
V(a,OUT) V(c,OUT)

.end
```

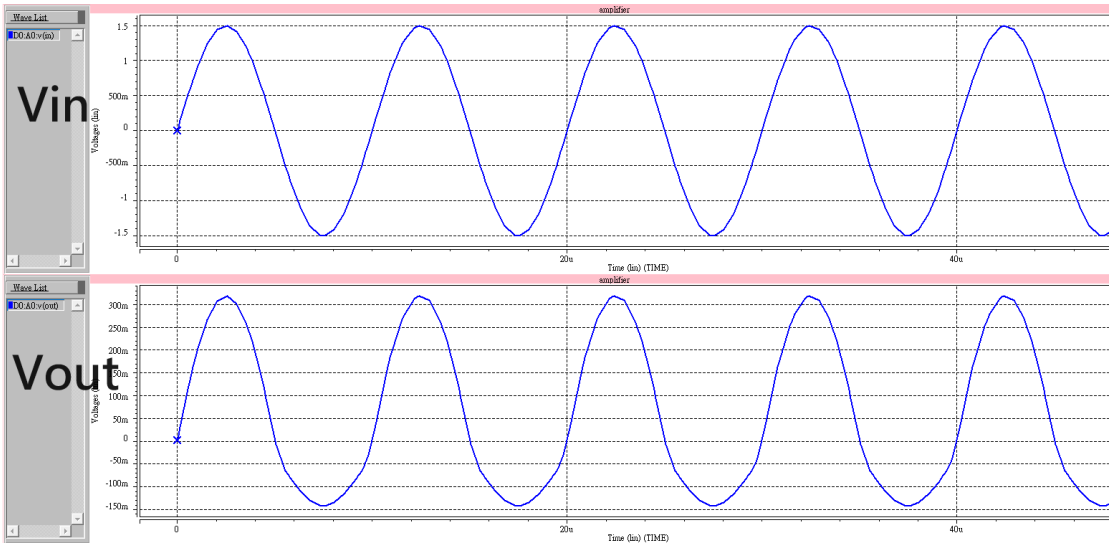

Fig. 37.2-2 The results of Experiment 37.2-**2**

Experiment 37.2-3 V1 Decreased from 3V to 2V

In this experiment, V1 is decreased from 3V to 2V. The program is in Table

37.3-3 and the results are in Fig. 37.3-3.

Table 37.3-3 The program for Experiment 37.3-3

```
amplifier
.protect
.lib "C:\model\tsmc\MIXED035\mm0355v.l" TT
.unprotect
.op
.options nomod post

V1   V1   0    2v
V2   V2   0    5v
V1p  V1p  0    -2v
V2p  V2p  0    -5v

R1   V2   a    5K
R2   V2p  c    5K

M1   b    a    OUT V2p  M2N6802      W=2u L=2u
M2   V2   a    b   V2p  M2N6802      W=4u L=2u
M1p       d    c   OUT V2   M2N6804      W=2u L=2u
M2p       V2p  c   d   V2   M2N6804      W=4u L=2u

MD1       V1   V1  b   V2p  M2N6802      W=4u L=2u
MD2       V1p  V1p d   V2   M2N6804      W=4u L=2u
MD3       a    a   IN  V2p  M2N6802      W=2u L=2u
MD4       c    c   IN  V2   M2N6804      W=2u L=2u

RL   OUT 0    50

.model M2N6802   NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
Vmax=0 Xj=0
+          Tox=100n Uo=600 Phi=.6 Rs=.1084 Kp=20.88   Vto=2 NSUB=1E15
+          Rd=1.163   Cbd=732p Pb=.8 Mj=.5 Fc=.5 Cgso=1.725n
+          Cgdo=136.7p   Is=1.823p N=1 Tt=2060n)

.model M2N6804   PMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
Vmax=0 Xj=0
```

```
+          Tox=100n Uo=300 Phi=.6 Rs=.153 Kp=10.46 Vto=-2 NSUB=1E15
+          Rd=66.52m    Cbd=1.281n Pb=.8 Mj=.5 Fc=.5 Cgso=1.798n
+          Cgdo=134.9p    Is=5.477p N=3 Tt=295n)

Vin   IN    0      sin(0V 1.5V 3K)

.tran 0.1us 0.6ms
.probe TRAN I(M1) I(M2) I(M1p) I(M2p) power=PAR('V(OUT)*I(RL)') V(a,b)

.end
```

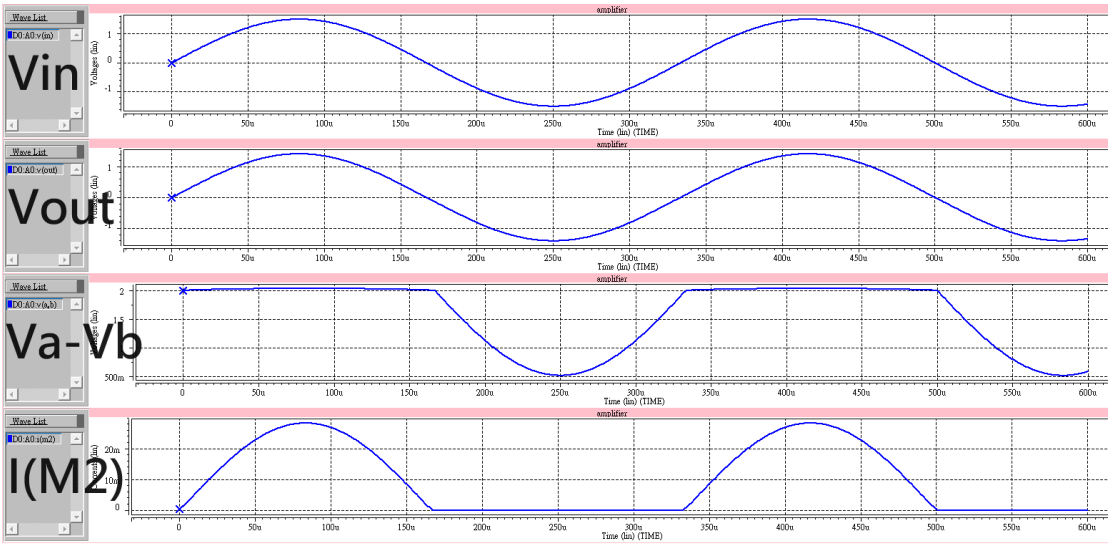

Fig. 37.3-3 The results of Experiment 37.3-3

From Fig. 37.3-3, we can see that when Vin is larger than 0, M2 conducts. This shows that the circuit does not behave as a Class G power amplifier. Note that V1=2V=Vth. Therefore, V1-Vth=2-2=0. According to Equation (37-7), in this case, M2 will conduct when Vin is larger than 0. Thus the amplifier is not a Class G power amplifier any more.

Experiment 37.2-4 Increasing Vin Amplitude from 1.5V to 4V.

In this experiment, the amplitude of Vin is increased from 1.5V to 4V. The program is in Table 37.2-4 and the results are in Fig. 37.3-4.

Table 37.2-4 The program for Experiment 37.2-4

```
amplifier
```

```
.protect
.lib "C:\model\tsmc\MIXED035\mm0355v.l" TT
.unprotect
.op
.options nomod post

V1   V1   0    3v
V2   V2   0    5v
V1p  V1p  0    -3v
V2p  V2p  0    -5v

R1   V2   a    5K
R2   V2p  c    5K

M1   b    a    OUT V2p  M2N6802      W=2u L=2u
M2   V2   a    b    V2p  M2N6802      W=4u L=2u
M1p       d    c    OUT V2   M2N6804      W=2u L=2u
M2p       V2p  c    d    V2   M2N6804      W=4u L=2u

MD1       V1   V1   b    V2p  M2N6802      W=4u L=2u
MD2       V1p  V1p  d    V2   M2N6804      W=4u L=2u
MD3       a    a    IN   V2p  M2N6802      W=2u L=2u
MD4       c    c    IN   V2   M2N6804      W=2u L=2u

RL   OUT 0    50

.model M2N6802   NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
Vmax=0 Xj=0
+          Tox=100n Uo=600 Phi=.6 Rs=.1084 Kp=20.88    Vto=2 NSUB=1E15
+          Rd=1.163    Cbd=732p Pb=.8 Mj=.5 Fc=.5 Cgso=1.725n
+          Cgdo=136.7p    Is=1.823p N=1 Tt=2060n)

.model M2N6804   PMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
Vmax=0 Xj=0
+          Tox=100n Uo=300 Phi=.6 Rs=.153 Kp=10.46 Vto=-2 NSUB=1E15
+          Rd=66.52m    Cbd=1.281n Pb=.8 Mj=.5 Fc=.5 Cgso=1.798n
+          Cgdo=134.9p    Is=5.477p N=3 Tt=295n)
```

```
Vin   IN    0      sin(0V 4V 3K)

.tran 0.1us 0.6ms
.probe TRAN I(M1) I(M2) I(M1p) I(M2p) power=PAR('V(OUT)*I(RL)') V(a,b)

.end
```

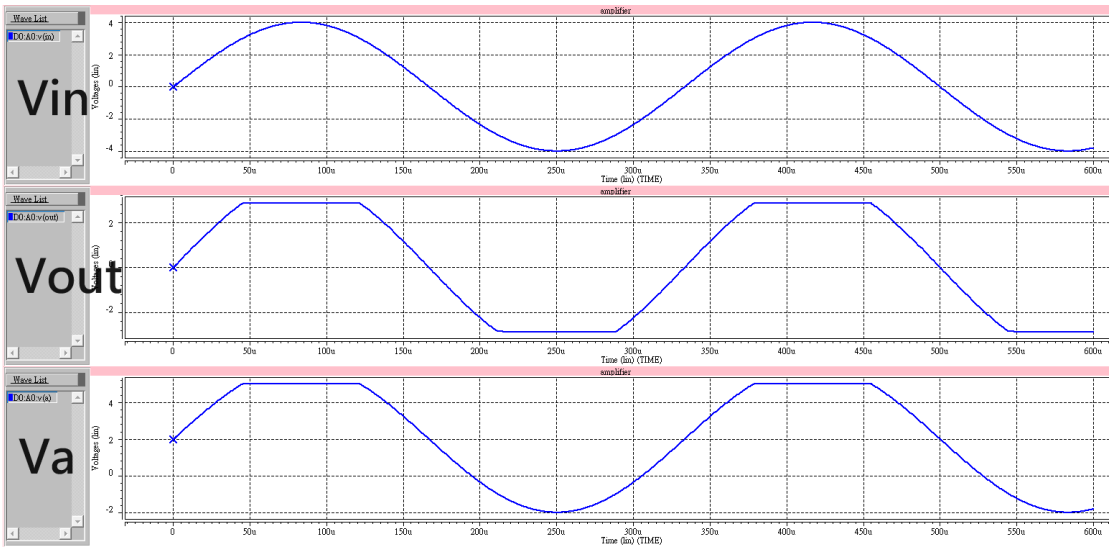

Fig. 37.2-4 The results of Experiment 37.2-4

From Fig. 37.2-4, we can see that the circuit does not work because Va is now equal to Vin+Vth=4+2=6V which is larger that V2. M2 becomes saturated.

Experiment 37.2-5 Increasing Vin Amplitude from 1.5V to 3V

In this experiment, we increased the Vin amplitude from 1.5V to 3V. The program is in Table 37.2-5 and the results are in Fig. 37.2-5.

Table 37.2-5 The program for Experiment 37.2-5

```
amplifier
.protect
.lib “C:\model\tsmc\MIXED035\mm0355v.l” TT
.unprotect
.op
.options nomod post

V1   V1   0     3v
```

```
V2   V2   0    5v
V1p  V1p  0    -3v
V2p  V2p  0    -5v

R1   V2   a    5K
R2   V2p  c    5K

M1   b    a    OUT V2p  M2N6802      W=2u L=2u
M2   V2   a    b   V2p  M2N6802      W=4u L=2u
M1p       d    c   OUT V2   M2N6804      W=2u L=2u
M2p       V2p  c   d   V2   M2N6804      W=4u L=2u

MD1       V1   V1  b   V2p  M2N6802      W=4u L=2u
MD2       V1p  V1p d   V2   M2N6804      W=4u L=2u
MD3       a    a   IN  V2p  M2N6802      W=2u L=2u
MD4       c    c   IN  V2   M2N6804      W=2u L=2u

RL   OUT 0    50

.model M2N6802   NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
Vmax=0 Xj=0
+          Tox=100n Uo=600 Phi=.6 Rs=.1084 Kp=20.88    Vto=2 NSUB=1E15
+          Rd=1.163    Cbd=732p Pb=.8 Mj=.5 Fc=.5 Cgso=1.725n
+          Cgdo=136.7p    Is=1.823p N=1 Tt=2060n)

.model M2N6804   PMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
Vmax=0 Xj=0
+          Tox=100n Uo=300 Phi=.6 Rs=.153 Kp=10.46 Vto=-2 NSUB=1E15
+          Rd=66.52m    Cbd=1.281n Pb=.8 Mj=.5 Fc=.5 Cgso=1.798n
+          Cgdo=134.9p    Is=5.477p N=3 Tt=295n)

Vin  IN   0    sin(0V 3V 3K)

.tran 0.1us 0.6ms
.probe TRAN I(M1) I(M2) I(M1p) I(M2p) power=PAR('V(OUT)*I(RL)') V(a,b)

.end
```

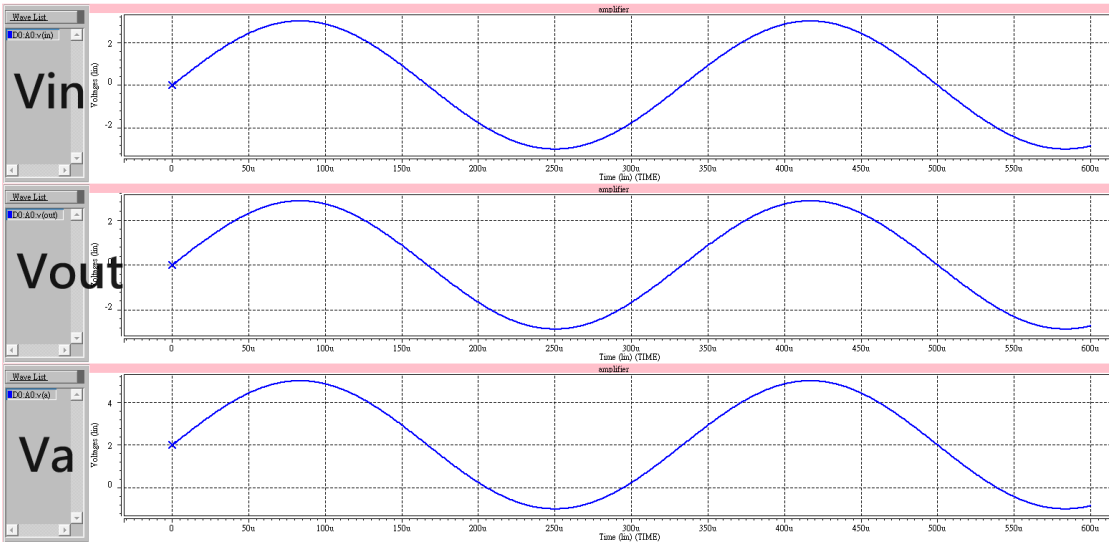

Fig. 37.2-5 The results of Experiment 37.2-5

We can see that the circuit works in this case. Note that Va = Vin + Vth = 3 + 2 = 5V which is exactly equal to V2. In the next experiment, we will show that the amplitude of Vin cannot be larger than 3V.

Experiment 37.2-6 Vin Amplitude Equal to 3.3V

In this experiment, Vin amplitude is 3.3V. The program is in Table 37.2-6 and the results are in Fig. 37.2-6. Since Va = Vin + Vth = 3.3 + 2 = 5.3V which is larger than V2, the circuit does not work.

Table 37.2-6 The program for Experiment 37.2-6

```
amplifier
.protect
.lib "C:\model\tsmc\MIXED035\mm0355v.l" TT
.unprotect
.op
.options nomod post

V1   V1   0    3v
V2   V2   0    5v
V1p  V1p  0    -3v
V2p  V2p  0    -5v
```

```
R1   V2   a    5K
R2   V2p  c    5K

M1   b    a    OUT V2p  M2N6802      W=2u L=2u
M2   V2   a    b    V2p  M2N6802      W=4u L=2u
M1p       d    c    OUT V2   M2N6804      W=2u L=2u
M2p       V2p  c    d    V2   M2N6804      W=4u L=2u

MD1       V1   V1   b    V2p  M2N6802      W=4u L=2u
MD2       V1p  V1p  d    V2   M2N6804      W=4u L=2u
MD3       a    a    IN   V2p  M2N6802      W=2u L=2u
MD4       c    c    IN   V2   M2N6804      W=2u L=2u

RL   OUT 0    50

.model M2N6802   NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
Vmax=0 Xj=0
+          Tox=100n Uo=600 Phi=.6 Rs=.1084 Kp=20.88    Vto=2 NSUB=1E15
+          Rd=1.163    Cbd=732p Pb=.8 Mj=.5 Fc=.5 Cgso=1.725n
+          Cgdo=136.7p    Is=1.823p N=1 Tt=2060n)

.model M2N6804   PMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
Vmax=0 Xj=0
+          Tox=100n Uo=300 Phi=.6 Rs=.153 Kp=10.46 Vto=-2 NSUB=1E15
+          Rd=66.52m    Cbd=1.281n Pb=.8 Mj=.5 Fc=.5 Cgso=1.798n
+          Cgdo=134.9p    Is=5.477p N=3 Tt=295n)

Vin  IN   0    sin(0V 3.3V 3K)

.tran 0.1us 0.6ms
.probe TRAN I(M1) I(M2) I(M1p) I(M2p) power=PAR('V(OUT)*I(RL)') V(a,b)

.end
```

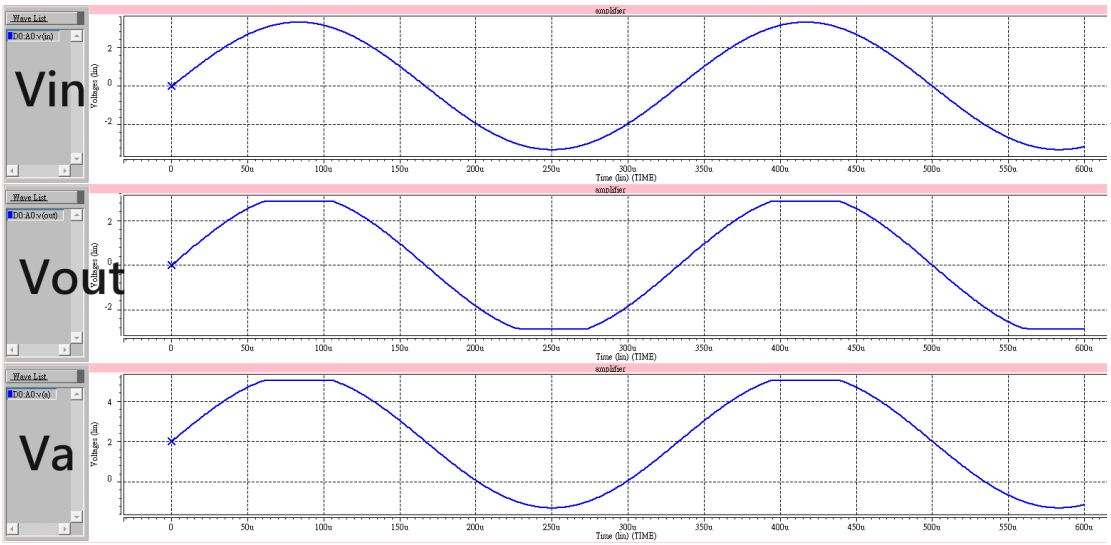

Fig. 37.2-6 The results of Experiment 37.2-6